

# Failure Analysis and Corrective Action in Wire Bonding of a Range Finder ASIC

K. S. R. C. Murthy

Society for Integrated circuit Technology and Applied Research Centre (SITAR), 1640, Doorvaninagar, Bangalore, Karnataka, India

**Abstract**— Failure associated with an aluminum wedge bonding in a range finder ASIC was analyzed. The proximity of guard ring and reduced pad size were found to cause rupture and shorting of wire bonds to the guard ring. With the help of thermosonic gold ball bonding the problem could be solved.

**Keywords**— wire bonding failure, CMOS guard ring, aluminum wedge bond, gold thermosonic ball bond

## I. INTRODUCTION

Following is a typical assembly and packaging flow to realize a hermetically sealed Mil Grade packaged Application Specific Integrated Circuit (ASIC) subsequent to wafer fabrication:

- 1] Wafer sort – Wafer Level Testing (ATS)
- 2] Inking bad dies – Ink dispensing
- 3] Wafer mounting - On dicing tape
- 4] Wafer Sawing – Dicing the wafer (Dicing machine)
- 5] Picking KGD (Known Good Die) and die attach
- 6] Wire Bonding
- 7] Optical Inspection
- 8] Lid sealing in nitrogen or dry air – Hermetic sealing
- 9] Package level functional testing
- 10] Marking

In the above flow, Non-Recurring Engineering (NRE) charges towards Step-1 (Wafer Sort) which involves probe card design, fabrication, test programme development, probing with a state of the art Automatic Test Equipment (ATE), debugging and Step-9 (Package level functional testing) which again involves test jig design, fabrication, test program development and testing with ATE are quite high compared to NRE as well as actual charges of other assembly and packaging activities. For a typical deliverable quantity of 100 or less devices the former NRE charges almost constitute 90% of overall cost. To avoid these high costs for prototype requirements, customers often prefer a blind-fold packaging in which dies are picked up randomly and packaged and tested directly at system level. This works out cheaper even at a package level yield of 30%.

This paper presents failure problems faced in such a blind fold packaging route with 0% yield at packaging level for one of the ASICs called range finder. The paper also analyses the failures and highlights corrective action taken to finally achieve 100% yield at packaging level.

## II. MATERIALS AND METHODS

The ASIC was designed in-house and fabricated on a silicon p/p+ epi-wafer using standard CMOS Fabrication technology. The wafer was subsequently mounted on a dicing tape after initial optical inspection and diced into individual dies with the help of ADT 7200 Dicing machine. Fig 1 shows a typical bare die.

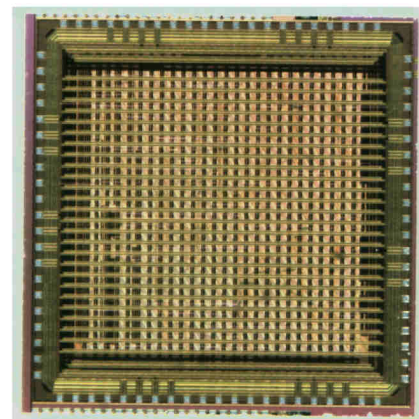


Fig. 1 Enlarged view of bare die of range finder ASIC

The die was subsequently bonded in an open tool 84 pin ceramic SOJ package procured from M/s Spectrum, US. Die attachment was done with Epotek E4110 two part silver epoxy and epoxy was cured at 150°C for 15 minutes. Wire bonding was done with the help of a K&S Aluminum Wedge bonder Model 1471 and aluminum wire was of 1 mil (25 micron thick). After visual inspection the package was hermetically sealed in a belt furnace (6 Zone Lindberg, GS) with combo lid and solder preform. The peak firing temperature was 330°C. Fig 2 shows the package after lid sealing.

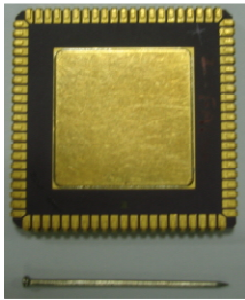


Fig. 2 Hermetically sealed range finder ASIC

The usual strategy is to package 5 devices initially including lid sealing and then carry out system level testing. After assessing the die yield batch level bonding and sealing were taken up. Following the same strategy initially five devices were packaged and sealed and tested at system level. This was followed by assembly and testing of 50 devices.

### III. RESULTS

When the initial five devices were subjected to system level testing, two out of five devices functionally passed completely. Accordingly it was presumed that the failure was due to intrinsic die level failure at wafer level fabrication.

Expecting a 40% yield after packaging, assembly of first batch of devices consisting 50 no. was taken up and were tested at system level after completion of assembly and packaging. It was found that all the devices failed at system level testing. Further analysis of test results revealed that the failure was mainly due to shorting. This was unexpected.

### IV. DISCUSSIONS

Aluminum wedge bonding is a well-established technology in SITAR Assembly House and thousands of devices were successfully assembled and delivered to customers over a decade. The package level yield loss never crossed 3%.

Among various bonding techniques employed in the IC industry the most popular techniques are Ultrasonic Aluminum wedge bonding and Thermosonic Gold wire Ball bonding. To understand the failures encountered in the present assembly and packaging of ASIC device, it would be helpful to briefly look into the advantages and constraints of both the wire bondings. Following is a brief discussion on both these bonding techniques in a CMOS ASIC Industry with advantages and disadvantages.

#### 4.1. Aluminum U/S Wedge Bonding:

Wedge bonding is named based on the shape of its bonding tool as shown in Fig 3.

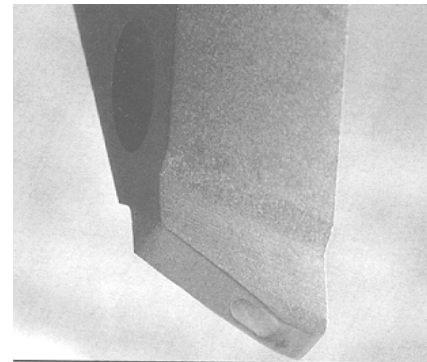


Fig 3. Wedge for Al wire wedge bonding (after K&S Micro-Swiss).

In this bonding, the wire is fed at an angle of 30-60° from the horizontal bonding surface through a hole in the back of bonding wedge. The first bond is made to the die pad and the second bond is made to the package pad (Ceramic substrate or Lead frame). This way edge shorts between the wire and die can be avoided. In the first bond the wire is pinned against the pad surface of the die and an U/S (Ultra Sonic) bond is performed. Next, the wedge rises and executes a motion to create a desired loop shape after which at the second bond location, the wedge makes a second bond at package pad. During the loop formation, the movement of the axis of the bonding wedge feed hole must be aligned with the center line of the first bond, so that the wire can be fed freely through the hole in the wedge. This directional constraint is one of the drawbacks or limitations of this bonding technique.

Typical scheme of wedge bonding is shown in Fig 4 and a typical wedge bonded device is shown in Fig 5 respectively.

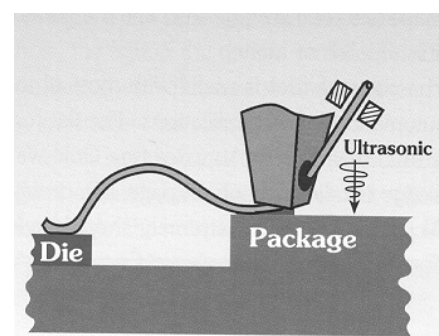


Fig 4 Ultrasonic wedge bonding (after K&S Micro-Swiss).

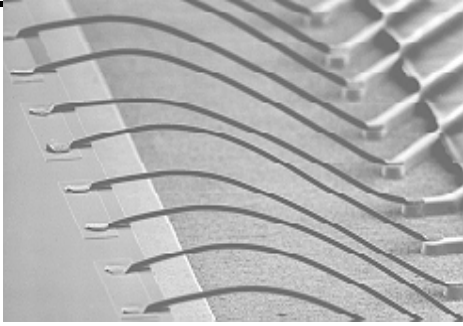


Fig 5. Application of wedge bonding from die pad to lead frame pad

The wedge bonding can be designed and manufactured to very small dimensions, down to 50  $\mu\text{m}$  pitch. Aluminum ultrasonic bonding is the most common wedge bonding process because of the low cost and the low working temperature. In addition, a wedge bond will give a smaller footprint than a ball bond.

#### 4.2. Gold Wire T/S Ball Bonding:

In this bonding technique, a gold wire passes through a hollow capillary and a small portion of the wire extending beneath the capillary is melted with the help of an electronic-flame-off system (EFO). Due to surface tension of the molten metal a ball is formed when the material solidifies. Fig 6 shows a typical capillary used in this technique.

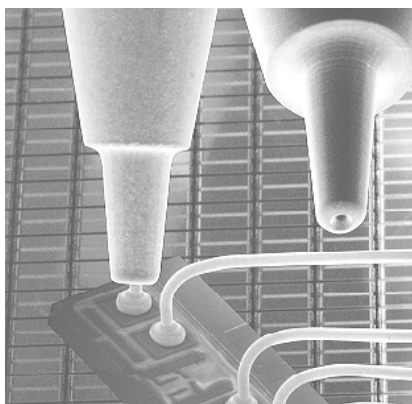


Fig 6. Capillary for ball bonding (after K&S Micro-Swiss).

During bonding the ball is pressed to the bonding pad on the die with sufficient force to cause plastic deformation and atomic inter-diffusion of the wire and the underlying metallization. This ensures an intimate contact between the two metal surfaces and forms the first bond (ball bond).

The capillary is subsequently raised and repositioned over the package bonding pad through a well-controlled and well-defined wire loop. The wire is then pressed against the package pad and with thermosonic energy and pressure second bond (wedge bond or stitch bond) is formed. This has a crescent or fishtail shape made by the imprint of the capillary's outer geometry. Then the wire clamp is closed, and the capillary ascends once again, breaking the wire just

above the wedge, an exact wire length is left for EFO to form a new ball to begin bonding the next wire.

Both thermal and ultra-sonic energies are used in achieving the interconnection and hence called Thermo Sonic Bonding. For the same reason, the bonding can be achieved at relatively low temperatures (150°C).

A typical Ball Bonding scheme is depicted in Fig 6 and Fig 7 shows a typical thermosonic ball bonded device.

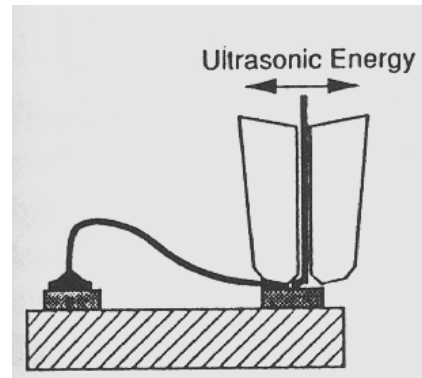


Fig 6. Thermosonic Ball bonding scheme.



Fig 7. Thermo Sonic ball bonding from die to lead frame

Ball bonding is generally used in application where the pad pitch is greater than 100  $\mu\text{m}$ .

#### 4.3. Wire Compositions and Metallurgical Systems in Bonding:

Gold and aluminum are the commonly used wire materials. Bonding these wires to different pad materials produces different metallurgical systems.

Since pure aluminum is too soft to be drawn into a fine wire, aluminum is often alloyed with 1% Si or 1% Mg to provide a strengthening mechanism.

Similarly ultra pure gold is very soft and hence small amounts of impurities such as 5-10 ppm by weight of Be or 30-100 ppm by weight of Cu are added to make the gold wire workable. Be-doped wire is stronger than Cu-doped wire by about 10-20% under most conditions, thus advantageous for automated thermosonic bonding where high-speed capillary movements generate higher stresses than in slow or manual bonders.

In wirebonding process, different pad metallizations are used, depending to the production requirements. Therefore, different metallurgical systems can be formed with different reliability behaviours. The typical metallurgical systems are:

#### 4.3.1. Au-Au system

Gold wire when bonded to a gold bond pad yields extremely reliable bond since interface corrosion, intermetallic formation, or other bond-degrading conditions do not arise. Even the strength of a poorly welded gold-gold bond increases in strength with time and temperature. Gold wire welds best with heat and thermosonic bonds Au-Au bonds can be easily and reliably made.

#### 4.3.2. Au-Al system

Though Au-Al welding system is the most commonly used in wirebonding process, if not controlled well, this bonding system can easily lead to formation of Au-Al intermetallic compounds and associated Kirkendall voids. Temperature accelerates the formation of the same and reduce time of the operational life. The possible intermetallic compounds include Au<sub>5</sub>Al<sub>2</sub> (tan), Au<sub>4</sub>Al (tan), Au<sub>2</sub>Al (metallic gray), AuAl (white), and AuAl<sub>2</sub> (deep purple). As indicated all these intermetallics are coloured. Initially AuAl<sub>2</sub> may form in the interface between gold and aluminum during bonding process even at room temperature and later may transform to other Au-Al compounds depending on the temperature, time and bonding configurations. Therefore, if not controlled well, this system can present a reliability problem.

#### 4.3.3. Al-Al system

The aluminum- aluminum wire bond system is extremely reliable because it is not prone to intermetallic formation and corrosion. Aluminum wire on aluminum metallization weds best ultrasonically, although a thermocompression bond can be produced by high deformation.

#### 4.4. Wirebonding pad and wire loop designs

Bonding pad and wire loop designs depend on the type of bonding and wire diameters used.

##### 4.4.1. Ball bonding:

For ball bonding the ball size is approximately 2 to 3 times the wire diameter, 1.5 times for small ball applications with fine pitches, and 3 to 4 times for large bond pad application.

Bond size should not exceed 3/4 of the pad size, about 2.5 to 5 times the wire diameter, depending on the geometry and moving direction of capillary during bonding.

While loop heights of 150 mm are now common, loop length should be less than 100 times the wire diameter. When wire lengths increase in cases such as with high I/Os to more than 5 mm, care should be taken so that suspend length of wire between the die and lead frame should not vertically sag or horizontally sway. This can lead to wire shorts in subsequent assembly and screening tests.

##### 4.4.2. Wedge bonding

Wedge bonding can yield stronger bonds even when the bond is only 2-3  $\mu\text{m}$  wider than wire diameter. Pad length must support the long dimension of the wedge bond as well as the tail while the pad's long axis should be oriented along the intended wire path. Bond pitch must be designed to maintain consistent distance between wires.

#### 4.5. Bonding parameters

Bonding parameters are extremely important because they control the bonding yield and reliability directly. The key variables for wire bonding include:

- Bonding force and pressure uniformity
- Bonding temperature
- Bonding time
- Ultrasonic frequency and power

The optimum conditions are to be arrived at and controlled based on wire type, pad metallization, and device configurations. Thus for every type of product, a series of bonding tests have to be performed by varying these parameters to set optimum bonding conditions.

#### 4.6. Typical Bonding Failures

Following are a couple of typical bonding failures that can lead to a short:

- Deformed wedge bonds with excessive deformation at the heel, or where the bond has damaged the surrounding passivation or semiconductor device circuitry
- Bonds with excessive large tails touching adjacent bond pads or surrounding metallization. These failures can be avoided by paying attention to following design and bonding guidelines:
- Gold ball bonds on the die or package post wherein the ball bond diameter should not be greater than 5 times the wire diameter.
- Gold ball bonds where the wire exit should be completely within the periphery of the ball.
- Gold ball bonds where the wire center exit should be within the boundaries of bonding pad.
- Ultrasonic wedge bonds on the die or package post should not be more than 3 times the wire diameter in width or more than 5 times the wire diameter in length.
- Wirebond tails should not extend or make contact with any unglassivated metallization.
- Wirebond tails should not extend more than two wire diameters in length.
- No wire should come closer than two wire diameters to unglassivated die area, or the package lid.

#### 4.7. Failure Identification:

To understand the shorting problem, ten numbers of failed devices were opened with the help of M/s Tessolve and inspected under an optical microscope at higher magnification (100X Objective). The inspection, as shown

in Fig 8 and 9 at different locations, revealed that while doing the wedge bond on the die pad, the tool has ruptured the passivation of ASIC and shorted to a metal line which was running all around the die periphery close to bonding pads.

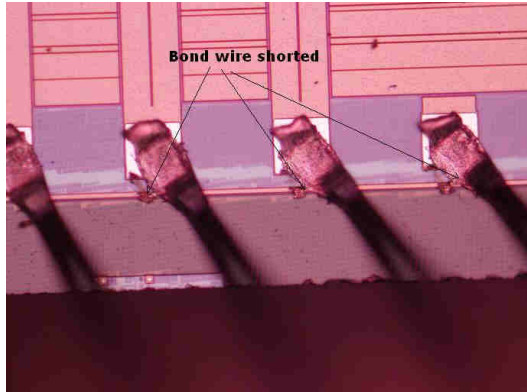


Fig 8. Ruptured wedge bonds shorting to metal line on ASIC on bottom side of the die

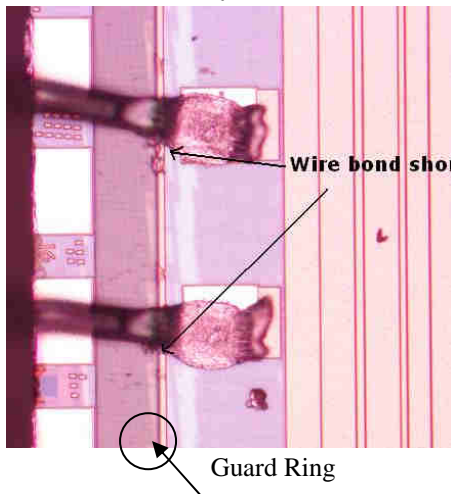
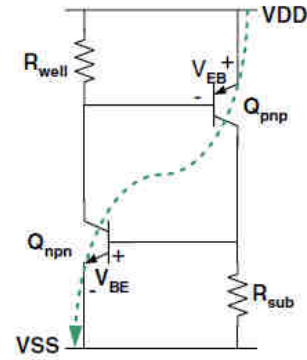
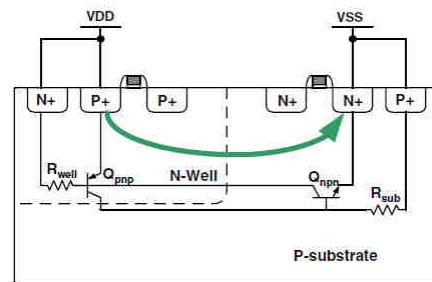


Fig 9. Ruptured wedge bonds shorting to metal line on ASIC on left side of the die

Some of the wedge bonds on die pad were found to be shorted to a metal line in the die. When explored further, it was found that the metal line running all around the die was a metal guard ring used as a standard for CMOS devices to avoid latch up problem. In CMOS circuits as shown in Fig 10, the field oxide and wells form two interconnected bipolar transistors.



(a)



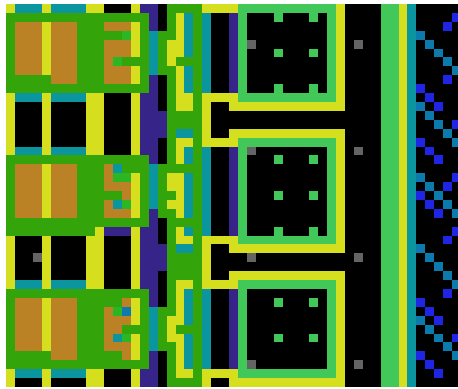
(b)

Fig 10. (a) Equivalent circuit of SCR path (b) cross-sectional view of the same in bulk CMOS device

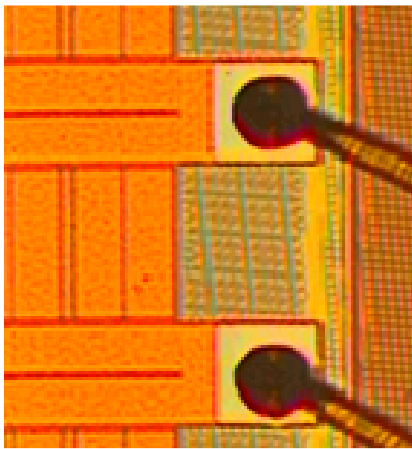
In CMOS integrated circuits, latch-up is formed by the parasitic SCR path between VDD and VSS. This parasitic path is inherent in the bulk CMOS ICs. When the SCR path is triggered on to conduct a huge current from VDD to VSS, the chip is often burned out. The first-order equivalent circuit of the SCR path is shown in Fig. 10(a), and the cross-sectional view of this path in a bulk CMOS technology is illustrated in Fig. 10(b) [1].

In order to prevent latch-up issue in bulk CMOS ICs, the guard ring structures and substrate/well pickups are often added to the I/O cells and internal circuits, respectively [2–4]. Guard ring structures are often applied to the I/O cell to prevent the latch-up in the bulk CMOS ICs.

Though the guard ring was a standard metal line and was used in all the CMOS ASICs fabricated earlier such a shorting problem was never faced previously. To analyze further the distance of guard ring from the die pads in the present ASIC was compared to the same in earlier ASICs. Fig 11 clearly shows that the guard ring in the present ASIC is closer compared to the one in previous ASICs.



(a)



(b)

Fig 11. Relative guard ring positions (a) Previous dies (b) Current Die.

When measured with Hisomet Union DH-T4 measuring microscope, the distance in the current ASIC was found to be  $13\mu\text{m}$  while it was  $40\mu\text{m}$  in previous ASICs.

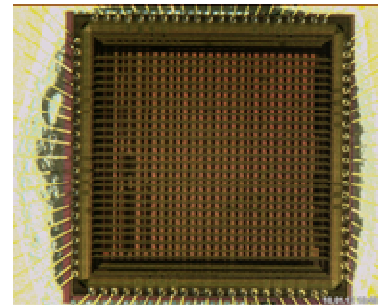
**4.8. Corrective Action:**

Due to smaller die pad and closer guard ring in the current ASIC and from all the bonding pad design calculations following conclusions have been arrived at:

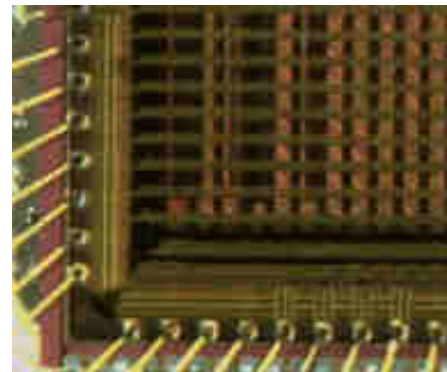
- $25\mu\text{m}$  dia Al wire cannot be used for this ASIC
- Even smaller  $18\mu\text{m}$  dia Al wire will be risky with wedge bonding. This is because with possible wedge length of 5 times wire dia i.e.  $90\mu\text{m}$  is longer than the total length of  $65\mu\text{m}$  die pad and  $13\mu\text{m}$  guard ring distance. This is likely to short the bond to the metal line.
- Only alternative appeared to be 18 thermo sonic ball bond. Even with maximum ball size of 3 X wire dia amounts to  $54\mu\text{m}$  and the bond will be within the pad with of have revealed that

Accordingly fresh dies were assembled by thermosonic ball bonding with  $18\mu\text{m}$  gold wire. Fig 13 shows thermosonically wire bonded die pads on all four sides of

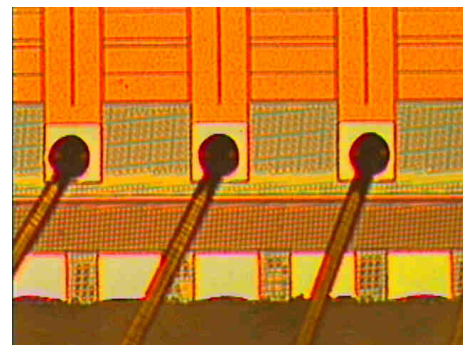
the wafer. Entire bonding was very clean. Also it may be noted that due to loop height adjustment wires have been taken up from die pad and then bonded to package pad so that at no place wire touches the die surface.



(a) Full wire bonded view



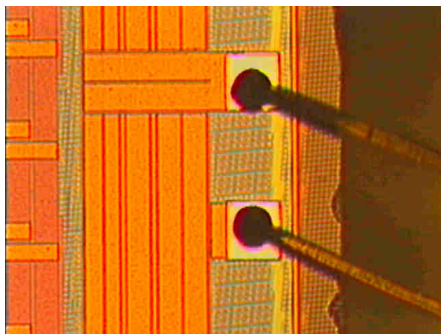
(b) Enlarged view



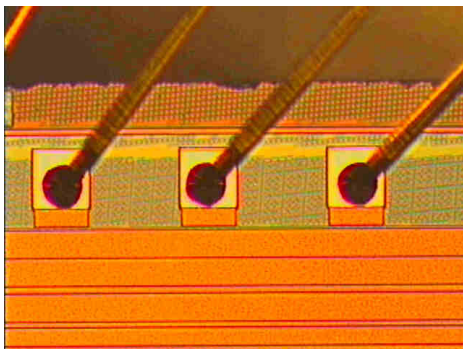
(c) Top view - Bottom side of die



(d) Side view



(e) Top view – right side of die



(f) Top view – top side of die



(g) Top view – left side of die

All the subsequent batches with above bonding technique have yielded 100% functionally passed devices. When subjected to MIL 883 screening as well as reliability tests no failures were observed.

## V. CONCLUSIONS

ASIC designer should consider the packaging issues while designing the ASIC. Designer should pay special attention to length of die pads and the separation of guard ring from the bonding pads. He should also be aware of type of bonding planned in the assembly house before freezing the design.

## ACKNOWLEDGEMENTS

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